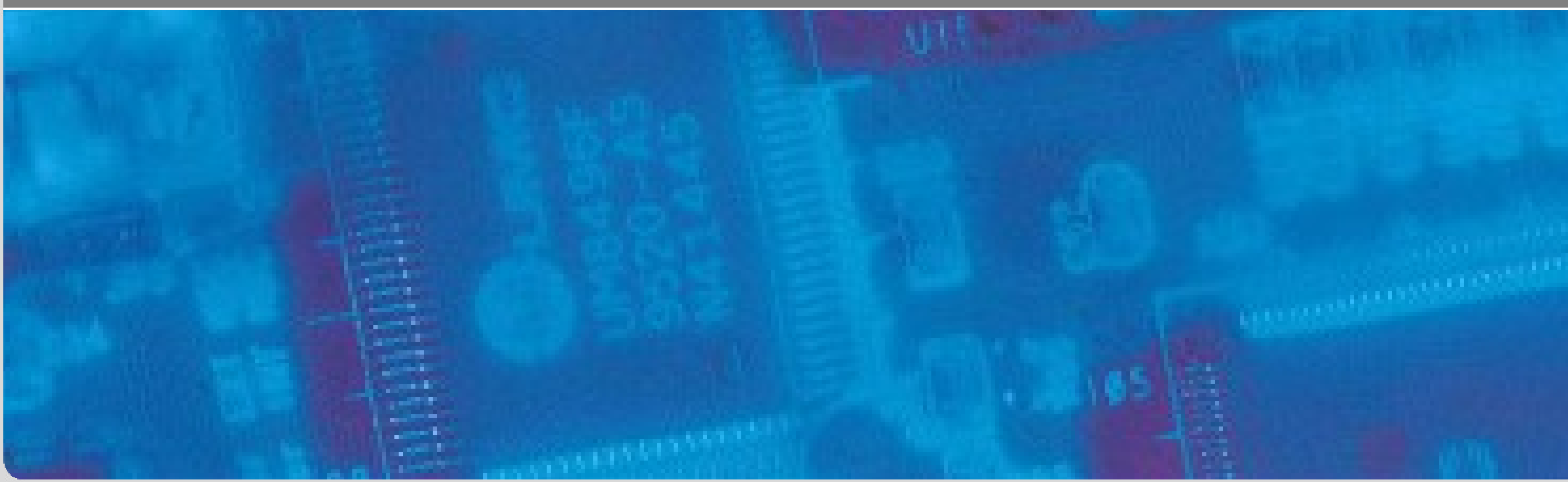
Low Power Design

Hussam Amrouch, Volker Wenzel on behalf of Prof. Dr. Jörg Henkel

Summer Term 2016

Karlsruhe Institute of Technology

CES – Chair for Embedded Systems



Lecture Slides

Karlsruhe Institute of Technology

Overview Low Power Design Lecture

- Introduction and Energy/Power Sources (1)
- Energy/Power Sources(2): Solar Energy Harvesting
- Battery Modeling – Part 1
- Battery Modeling – Part 2
- Hardware power optimization and estimation – Part 1
- Hardware power optimization and estimation – Part 2
- Hardware power optimization and estimation – Part 3
- Low Power Software and Compiler
- Thermal Management – Part 1
- Thermal Management – Part 2
- Aging Mechanisms in integrated circuits
- Lab Meeting

Agenda

- Introduction of Theoretical Background (Volker)
- Lab Demo (Hussam)

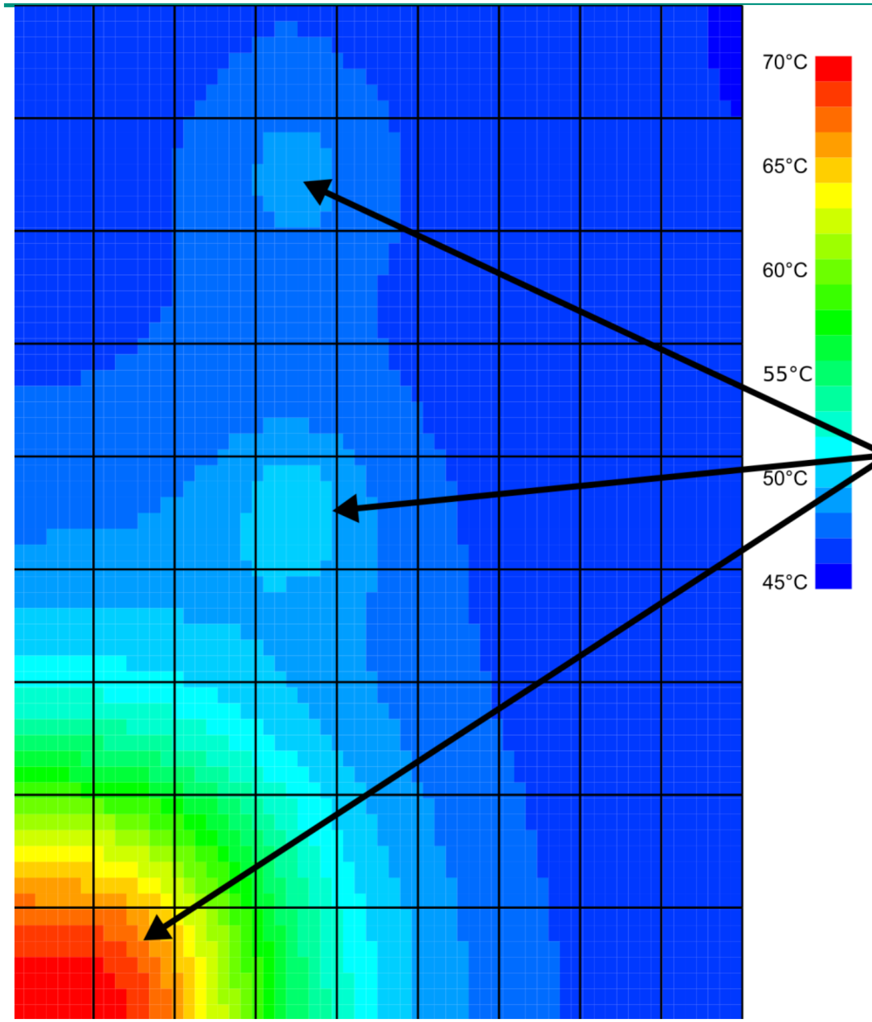
Means for Temperature Analysis

- Thermal Simulation
  - estimate thermal profile from power trace in different of blocks (e.g. using HotSpot)
- Thermal Sensor
  - hard sensor (e.g. thermal diode)
  - soft sensor (e.g. ring oscillator)
- Thermal Camera
  - very accurate reading
  - Thermal image shows actual temperature distibution across chip

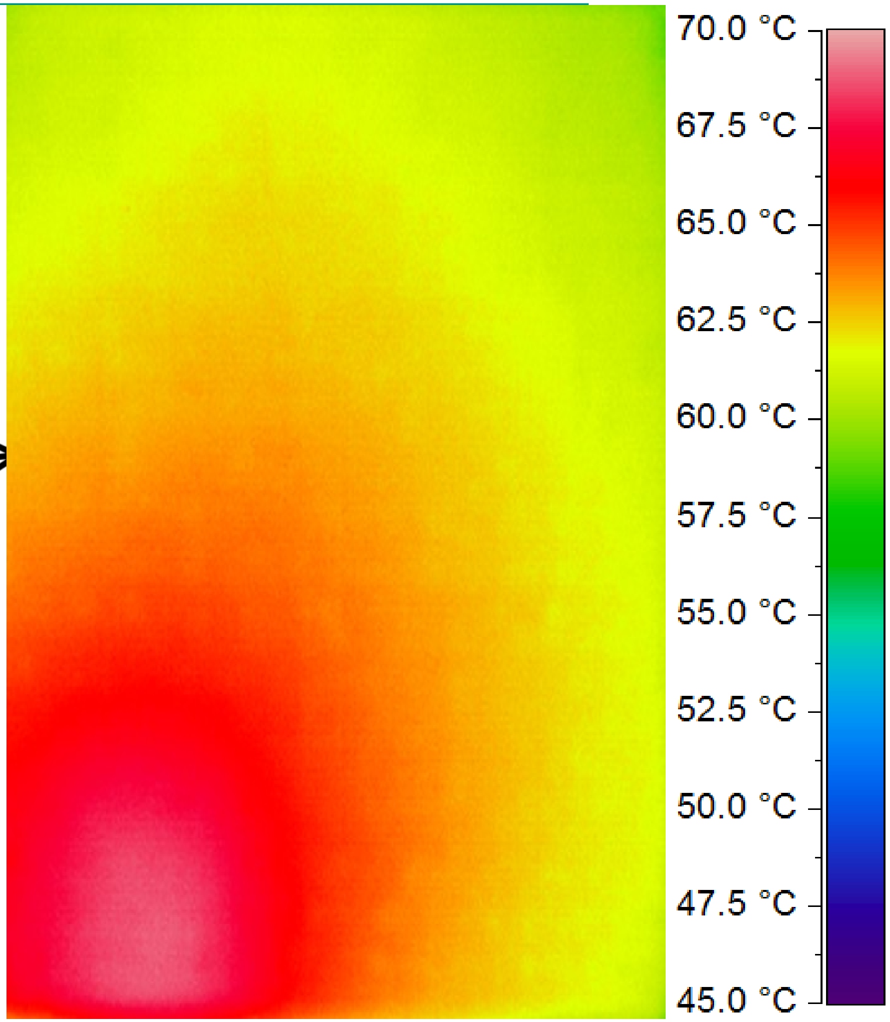
HotSpot vs. Measurement

- comparison of HotSpot and measurement w/ thermal camera (next slide)
- issues w/ on-chip sensors
  - calibration
  - chip area
  - gradients, inhomogeneous heat distribution; thermal diode might measure the wrong spot of the chip
- thermal camera superior way of measuring temperature

HotSpot Simulation of FPGAs



simulated thermal image



infrared image from the thermal camera

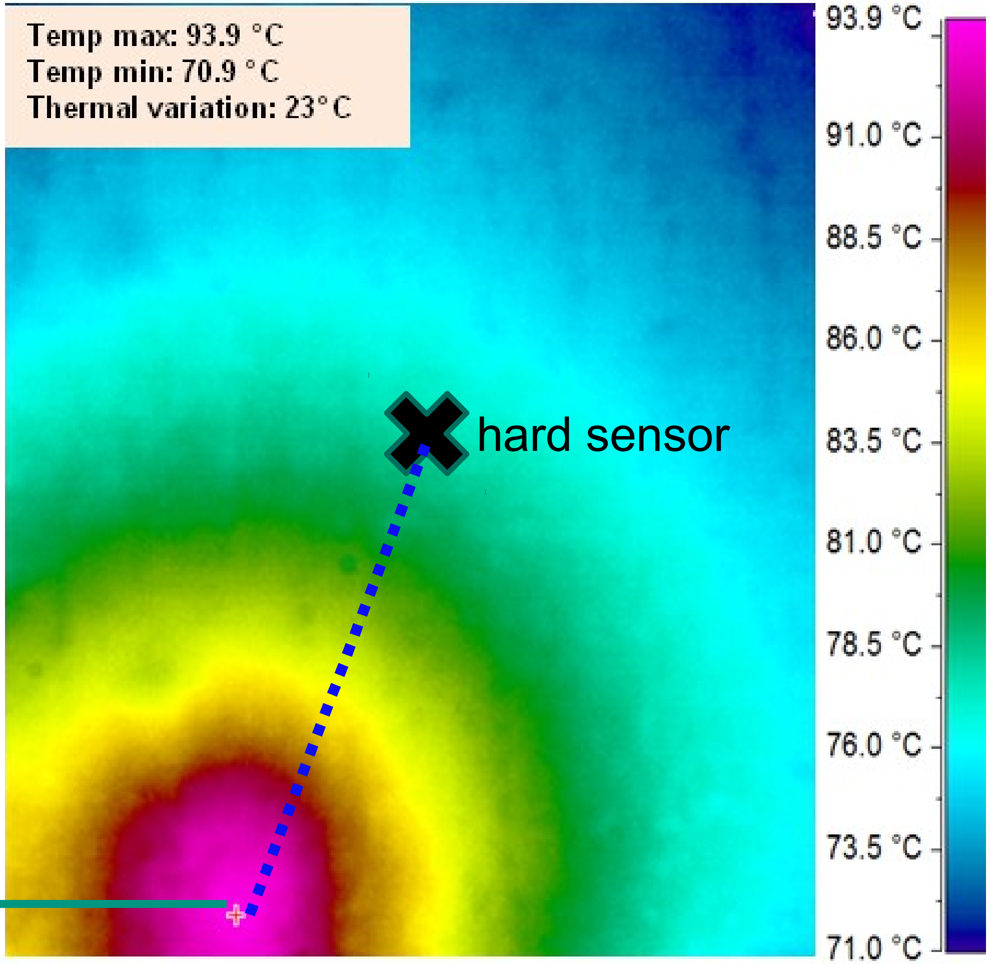
src: H. Amrouch et. al, “Analyzing the thermal hotspots in FPGA-based embedded systems,” FPL, 2013.

Hard Thermal Sensors

More than 10°C difference between the reading of sensor and the real peak temperature.

The potential hotspot reaches 94°C and is located at the corner of chip

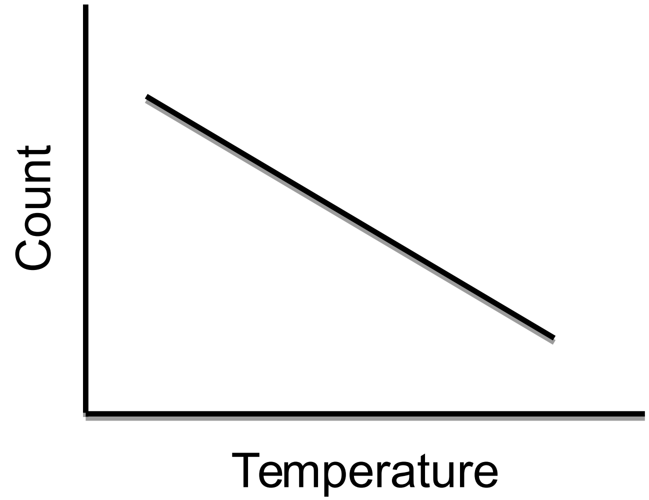
Src: H. Amrouch, J. Henkel

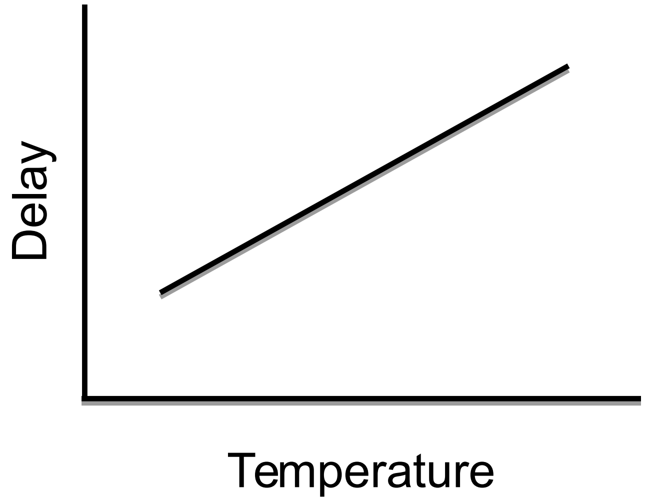


Xilinx Virtex-5, 65nm

Soft Thermal Sensors

- Soft sensors (e.g. ring oscillator):
  - \+ low power consumption
  - \+ low area overhead
    → Many can be placed across the chip
  - \- requires calibration (e.g. central hard sensor)





Thermal behavior in FPGA

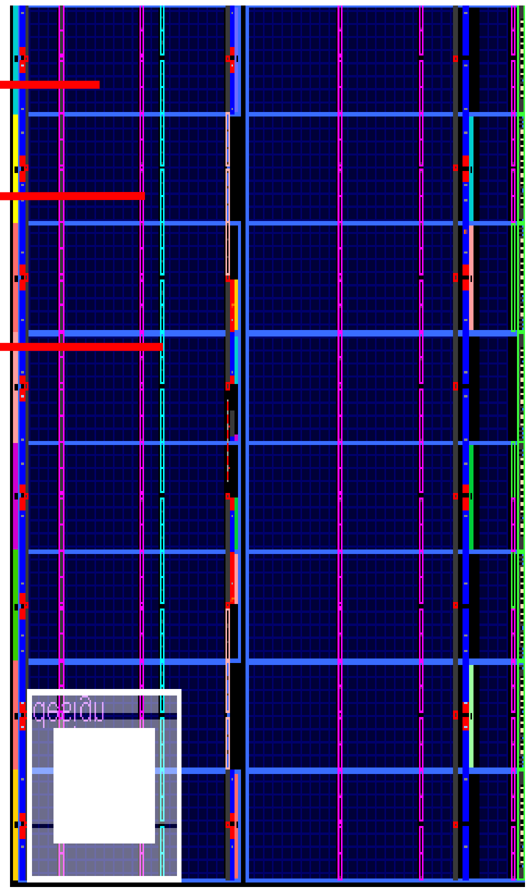
LUTs/FFs

BRAM Blocks

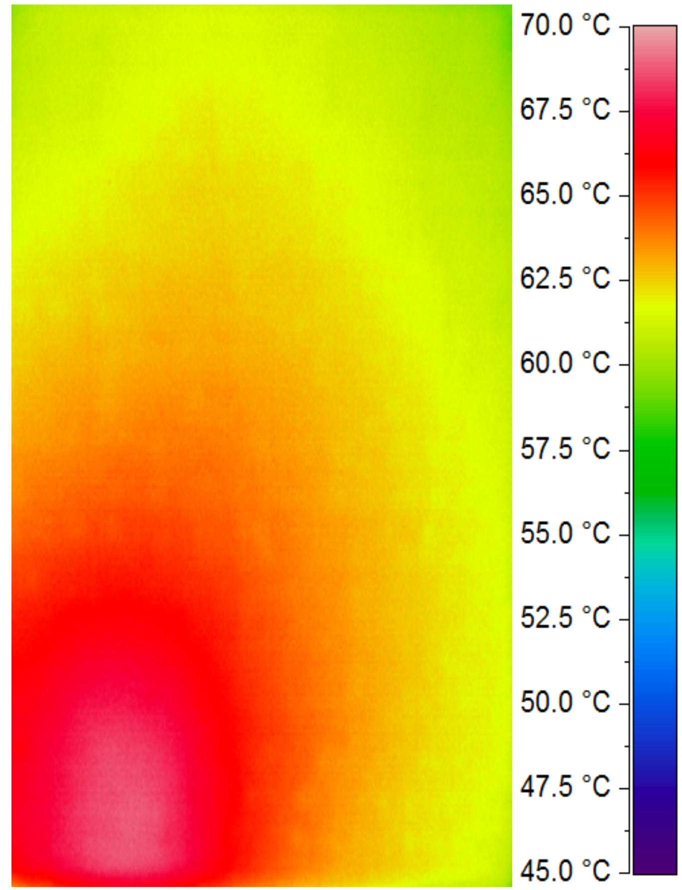
DSP Blocks

Resource	Available
SLICEL	884
SLICEM	340
DSP	12
BRAM	12

Tested region properties

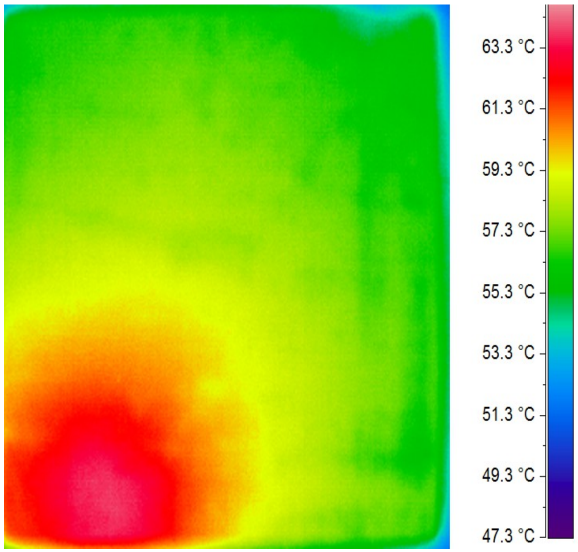


FPGA Floorplan (Xilinx Virtex-5)

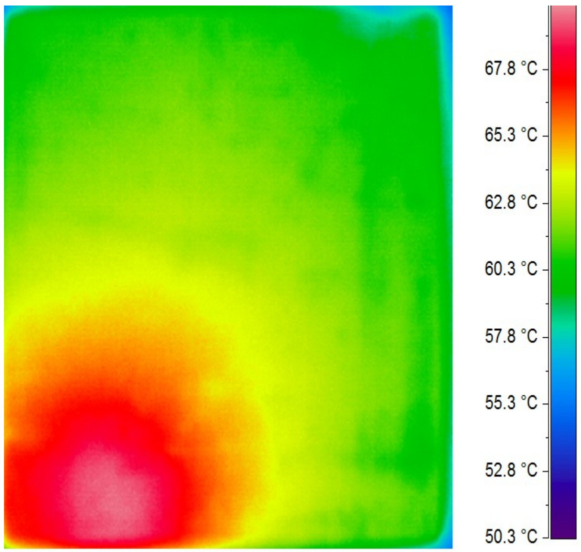


Infrared image obtained from our thermal setup

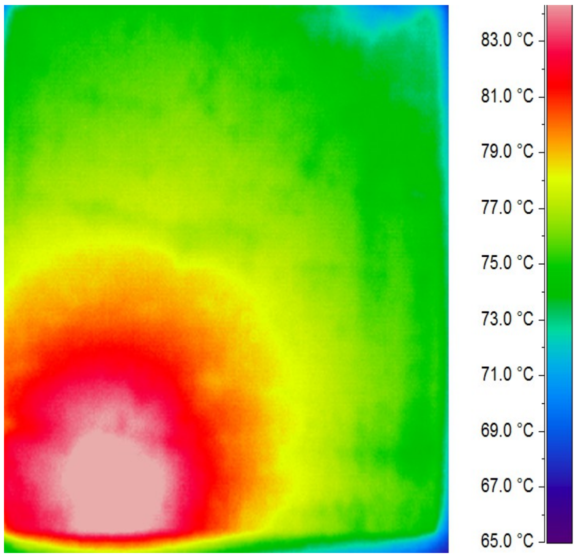
Thermal Behavior for Different FPGA Resources



Design: Only-Slices
Peak Temp = 64°C
Thermal variation = 13°C



Design: Slices+BRAMs
Peak Temp = 70°C
Thermal variation = 15°C



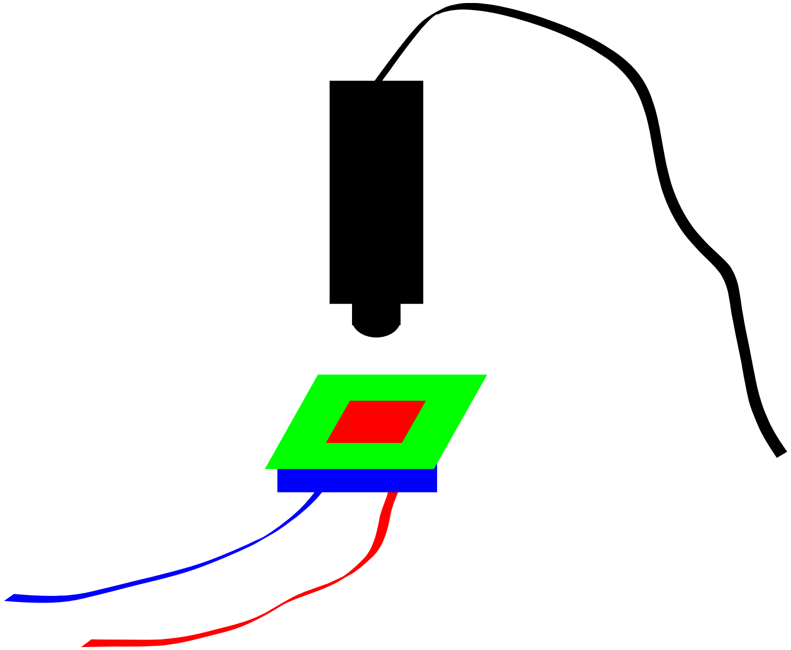
Design: Slices+BRAMs+DSPs
Peak Temp = 86°C
Thermal variation = 19°C

Slices = LUTs + FFs, ambient temp = 30°C

Src: H. Amrouch, J. Henkel

Thermal Setup

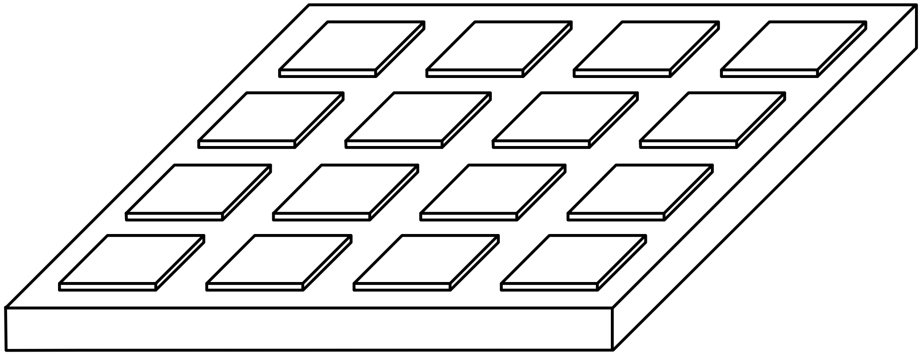
- need to remove packaging from chip
- alternative approach: IR-oil



Which chips are suitable for the thermal setup?

- ***c**ontrolled **c**ollapse **c**hip **c**onnection* (C4) aka **Flip Chips**
- bare silicon must be visible with packaging removed

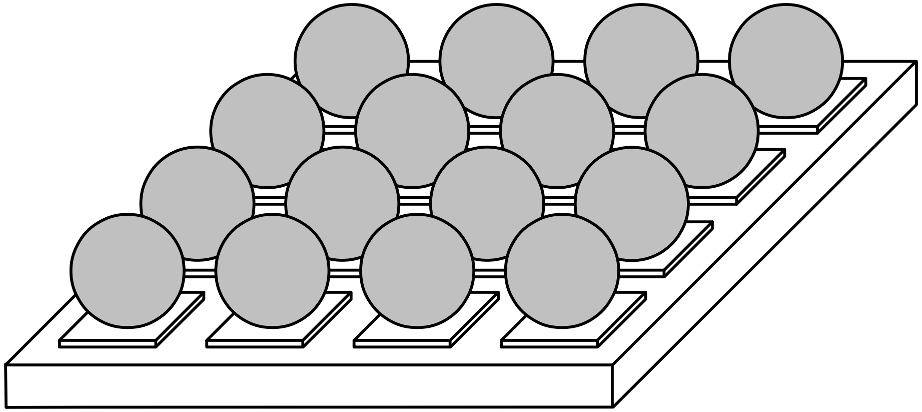
Fabrication of Flip Chips



Integrated circuits are created on the wafer

src:en.wikipedia.org/wiki/Flip_chip

Fabrication of Flip Chips



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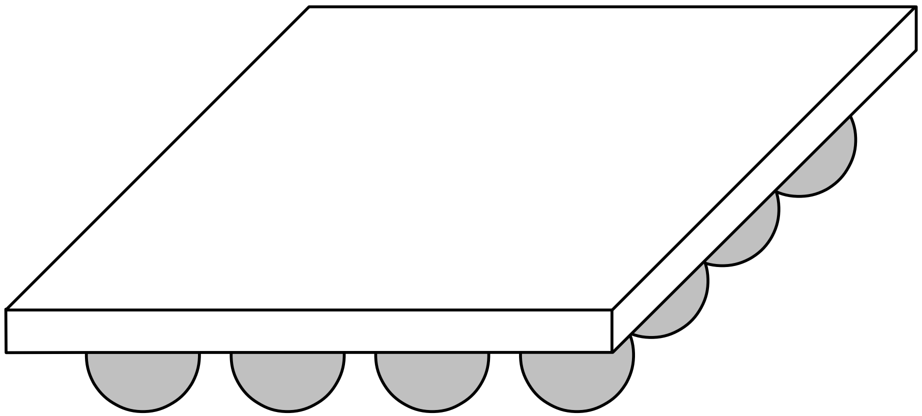
Fabrication of Flip Chips



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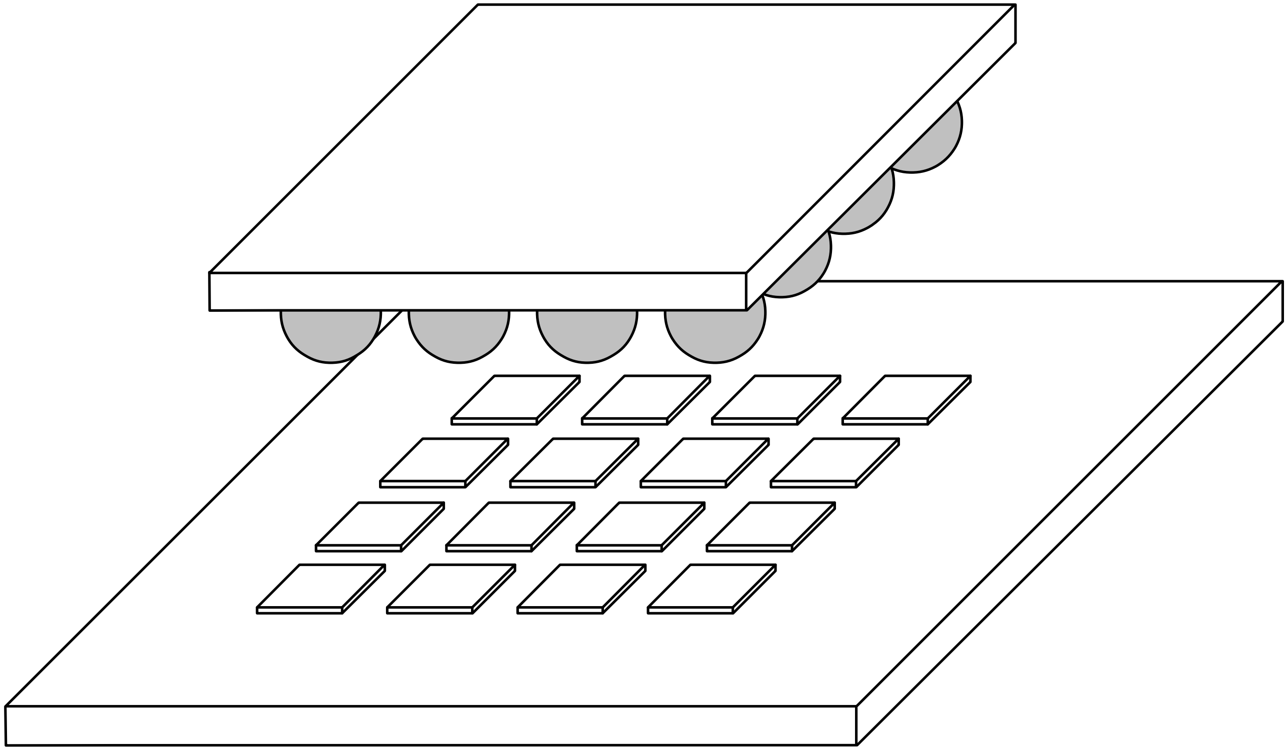

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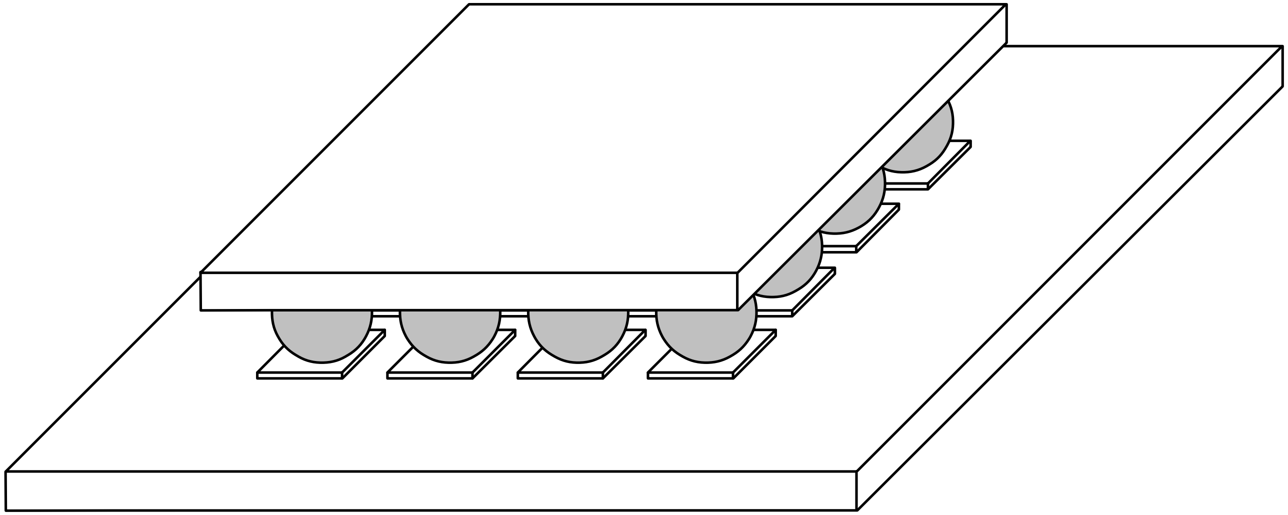
Fabrication of Flip Chips



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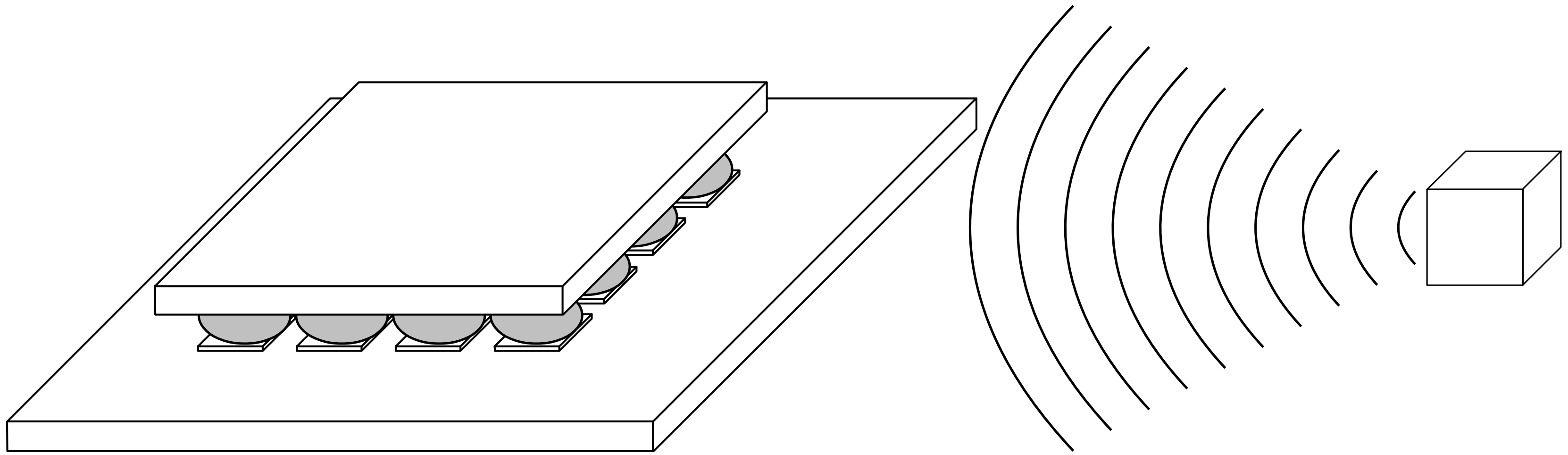
Fabrication of Flip Chips



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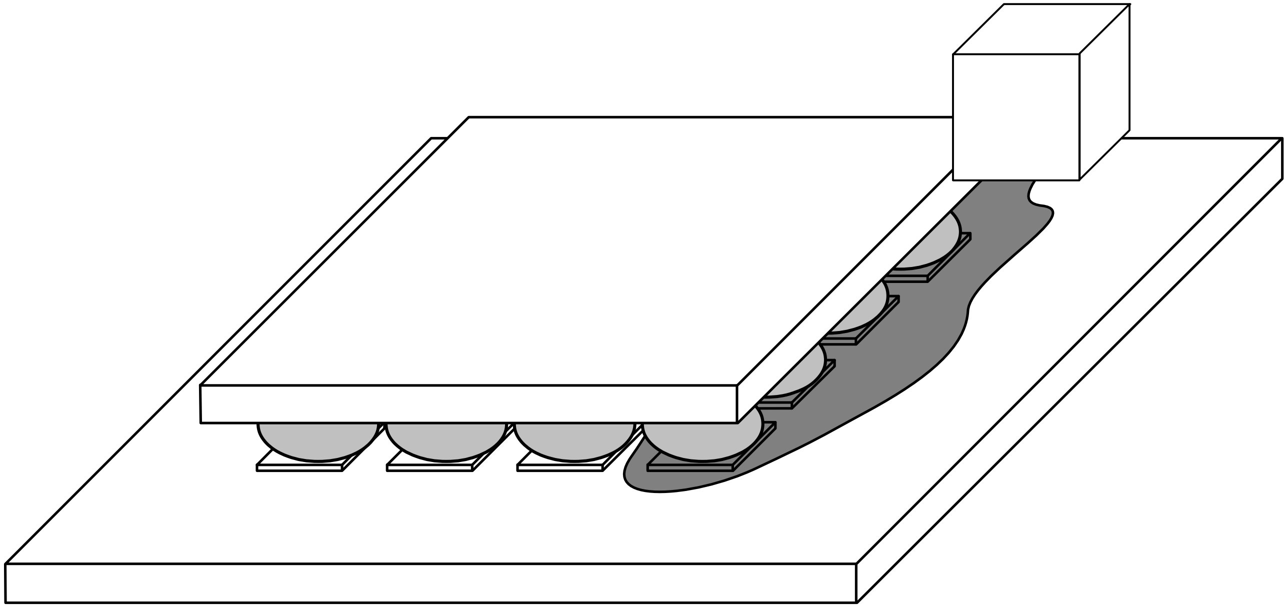

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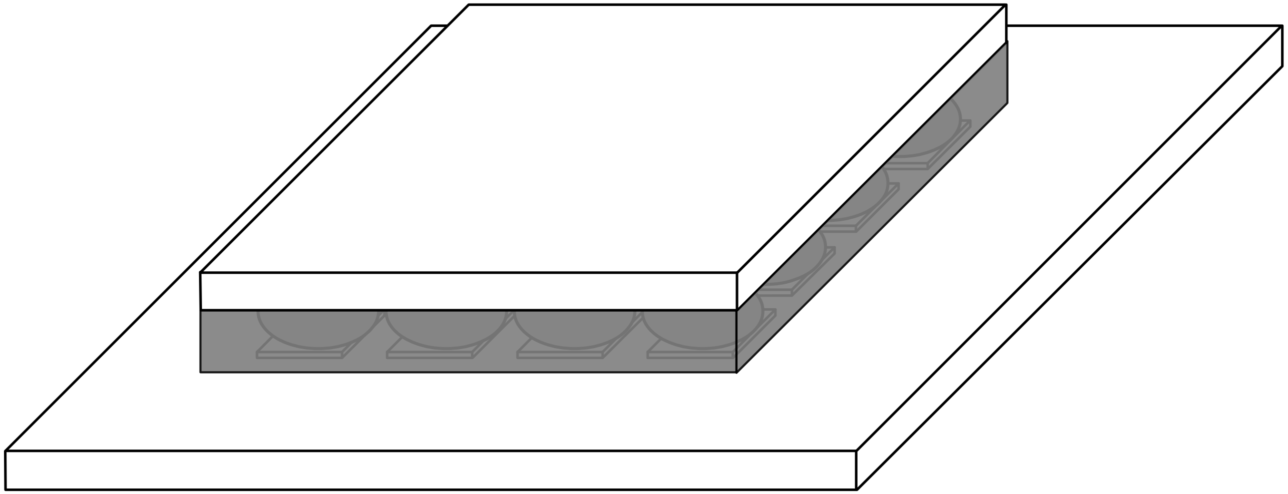
Fabrication of Flip Chips



src:en.wikipedia.org/wiki/Flip_chip

Thermal Camera

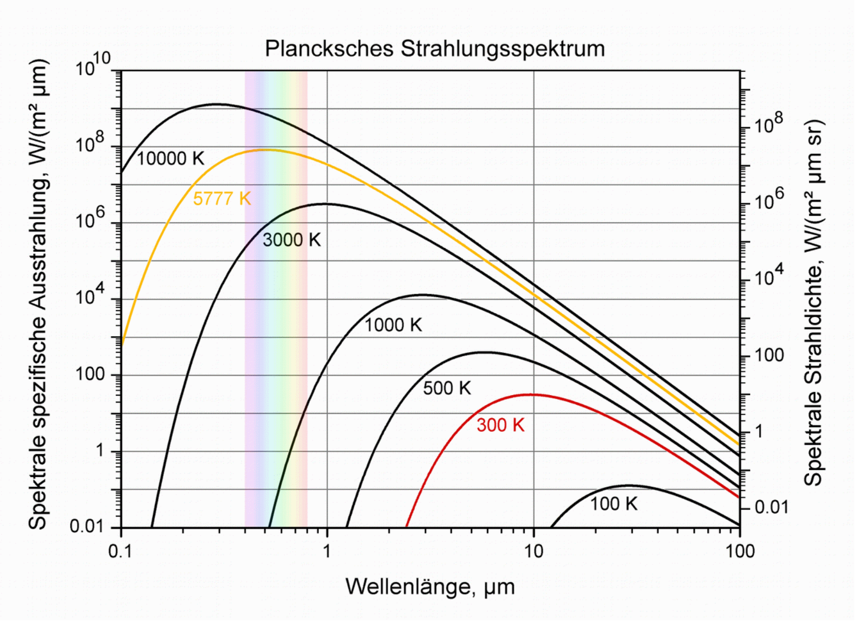
- infrared camera
- 8µm-14µm
- precise, contact-less temperature measurement

DIAS PyroView 380L compact
src: DIAS

Thermal Radiation

- hot bodies radiate!
- spectrum is characteristic of equilibrium temperature
- infrared for usual temperatures

$$P = \sigma A T^4$$

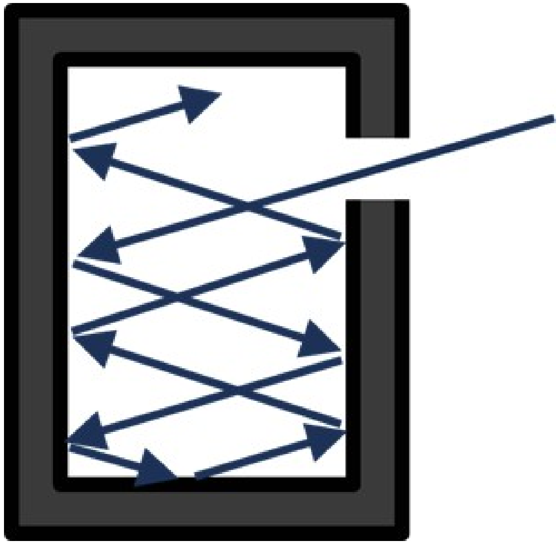


$$B_\lambda(T) = \frac{2hc^2}{\lambda^5} \frac{1}{e^{\frac{hc}{\lambda k_B T}} - 1}$$

src:en.wikipedia.org

Black Bodies

- idealized physical body
- absorbs all incident radiation
- is in thermal equilibrium
- optimal diffuse emitter

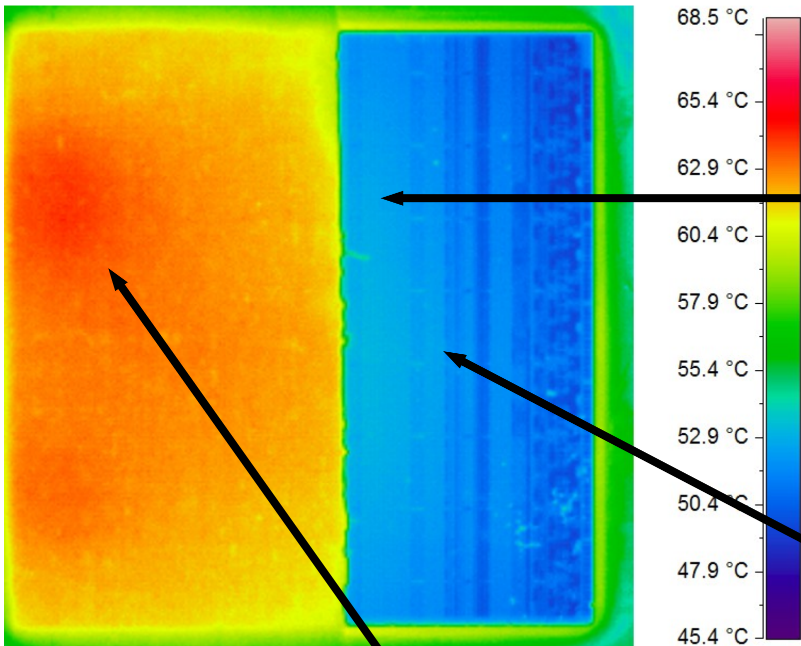


- real bodies: emissivity ε
- = energy emitted / energy emitted by black body at the same temperature
- ε between 0 and 1

src:en.wikipedia.org/wiki/Black_body

Emissivity Problem

Src: H. Amrouch, J. Henkel



Surface of silicon wafer with a low emissivity (~0.7) leads to inaccurate measurements. Reflection from surroundings seriously impacts the measured heat.

Structure of BRAM blocks appear more clearly without the masking tape

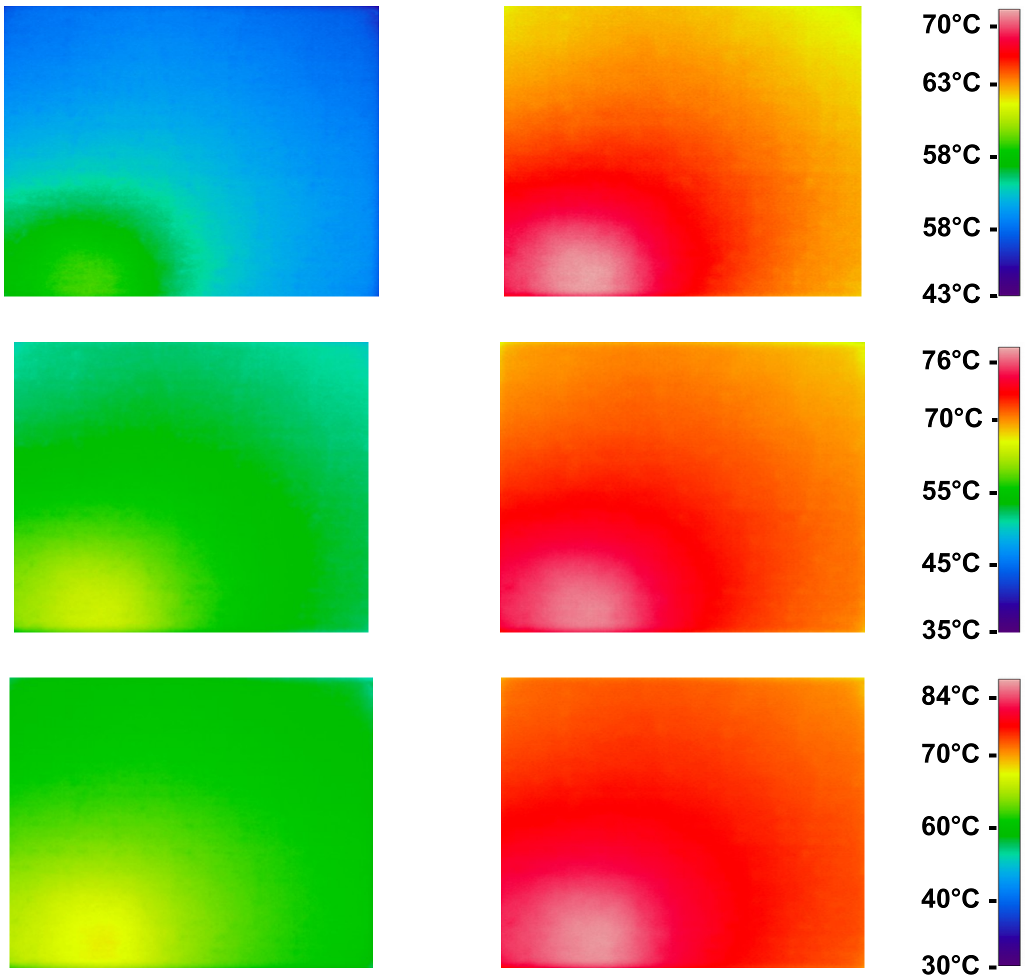
Masking tape with an emissivity of 0.9 coating the left half of chip shows that the temperature here is more closer to the actual one.

The variation in temperature between the right and left half is around 20°C

Impact of ambient temperature

Ambient Temperature: 20°C

Ambient Temperature: 30°C



Design: FFs/LUTs

Design: FFs/LUTs + BRAM blocks

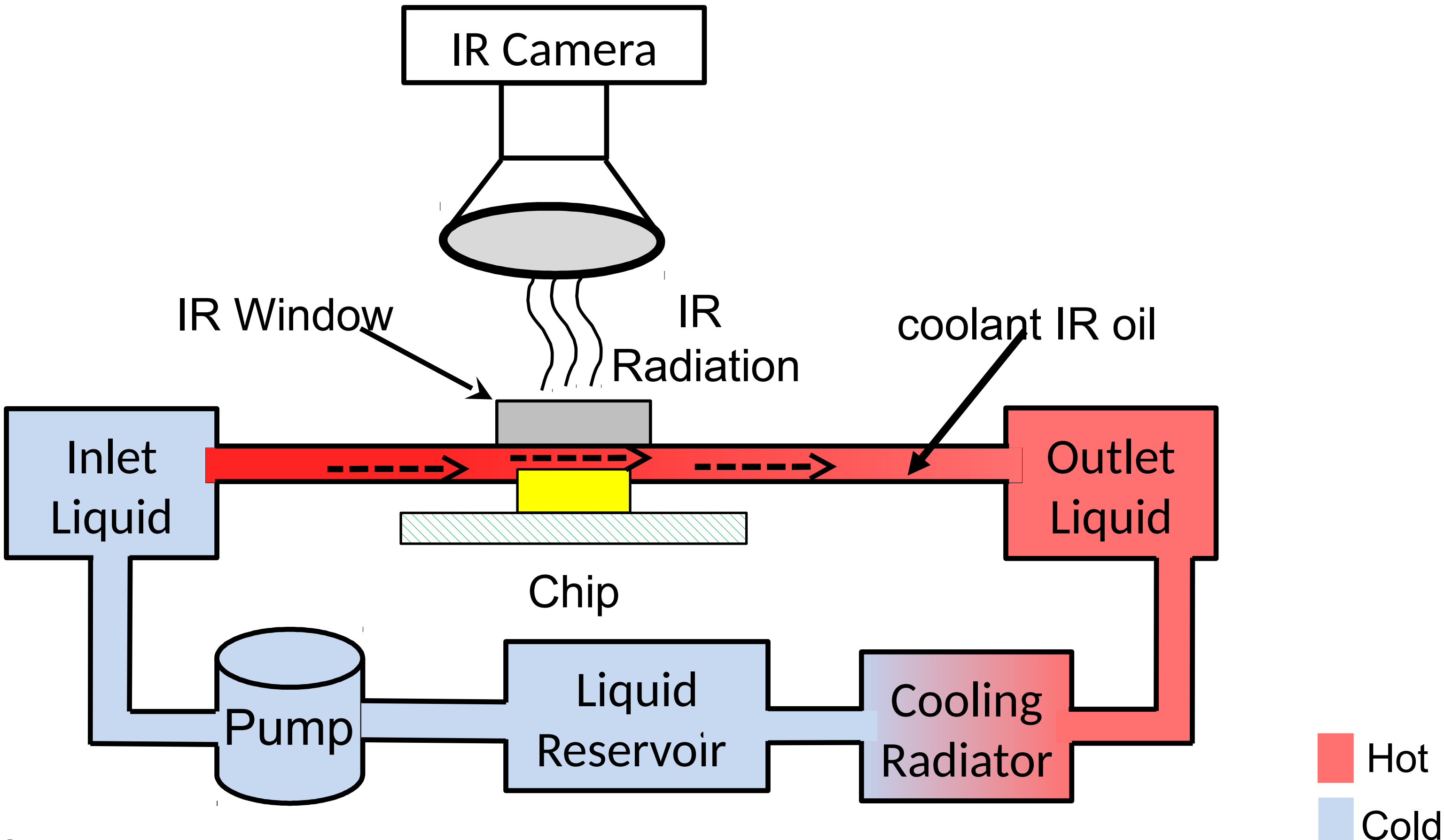
Design: FFs/LUTs + BRAM blocks + DSPs

src: H. Amrouch, J. Henkel

IR Thermography of Processors

- Major Challenge: Constructing IR-transparent cooling that
  - allows the IR radiation emitted from the chip to reach the thermal camera.
  - prevents the chip from burning up.

IR Thermography: State-of-the-Art



Src: H. Amrouch

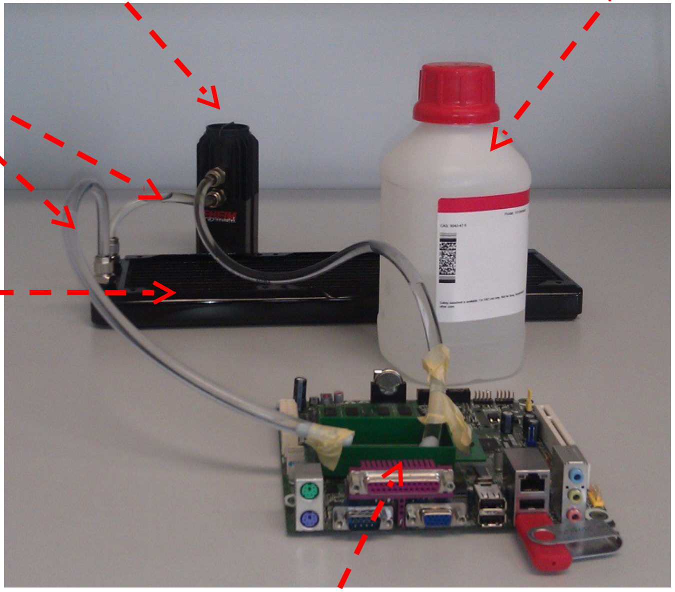
IR Thermography: State-of-the-Art

Pump

IR-transparent Oil

in/out tubes for oil

Radiator to cool the oil

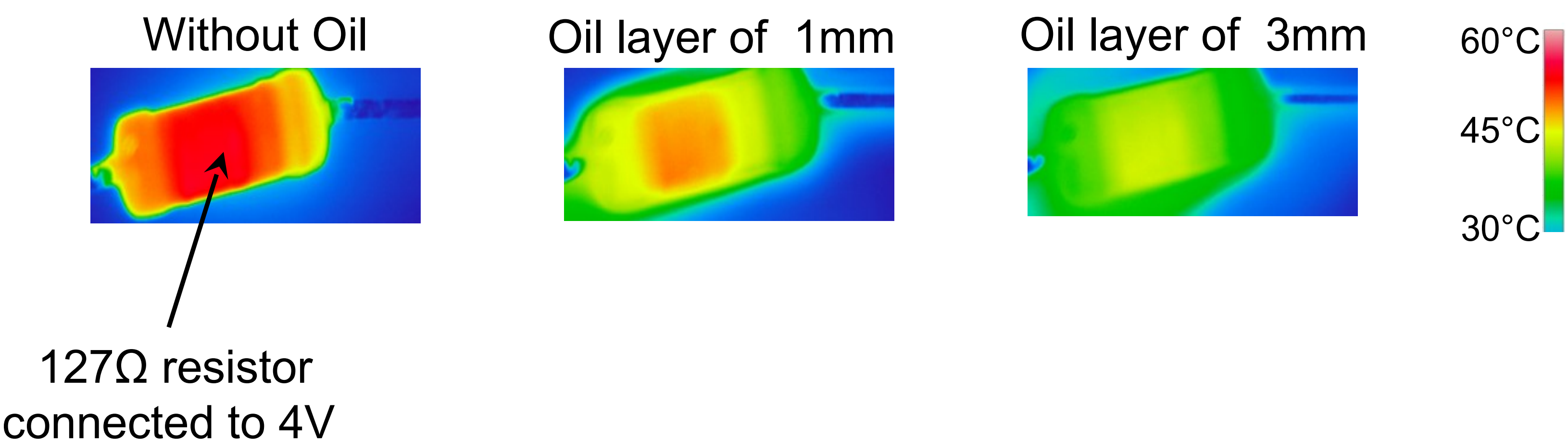


Opened chip (i.e. bare silicon)

Liquid-based Cooling Technique

Src: H. Amrouch

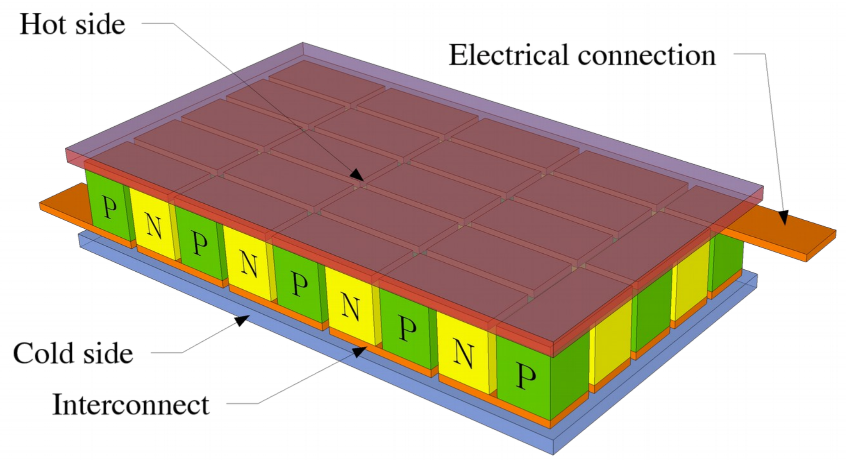
Impact of Oil

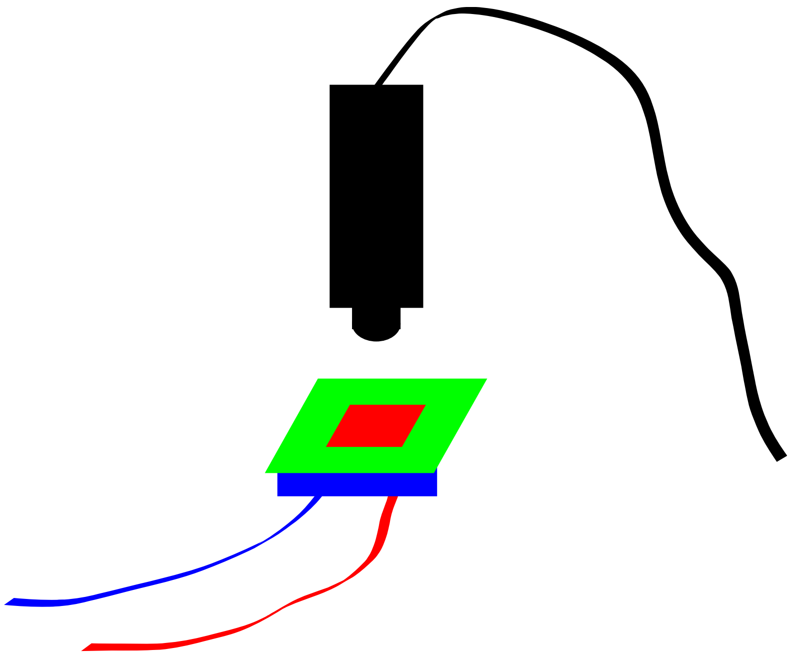


Thermal convection destroys the clarity of the captured IR images

Src: H. Amrouch

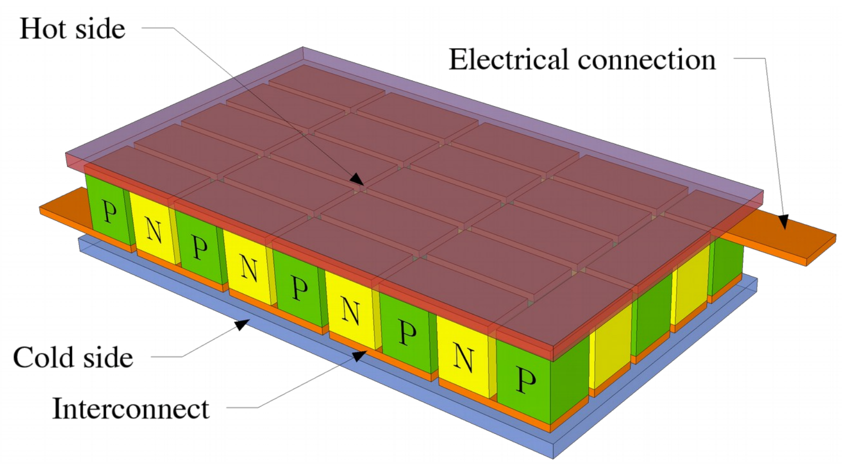
Thermoelectric Cooling

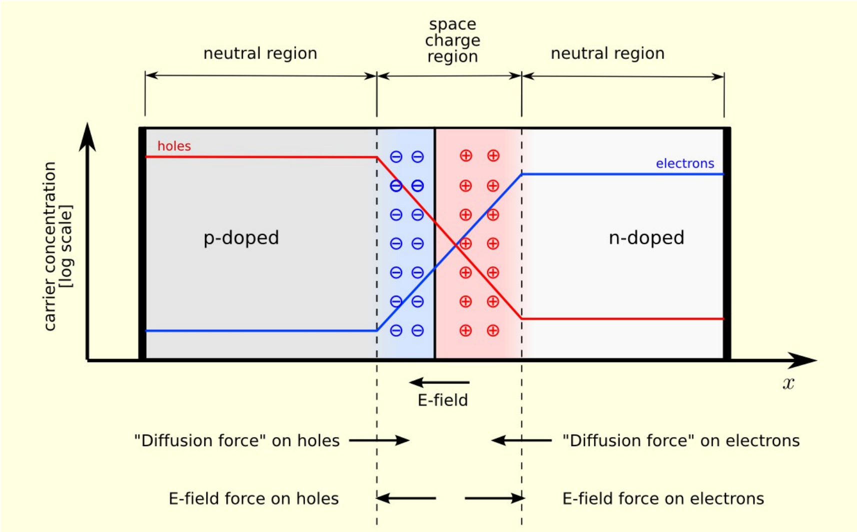




src:en.wikipedia.org

Thermoelectric Cooling

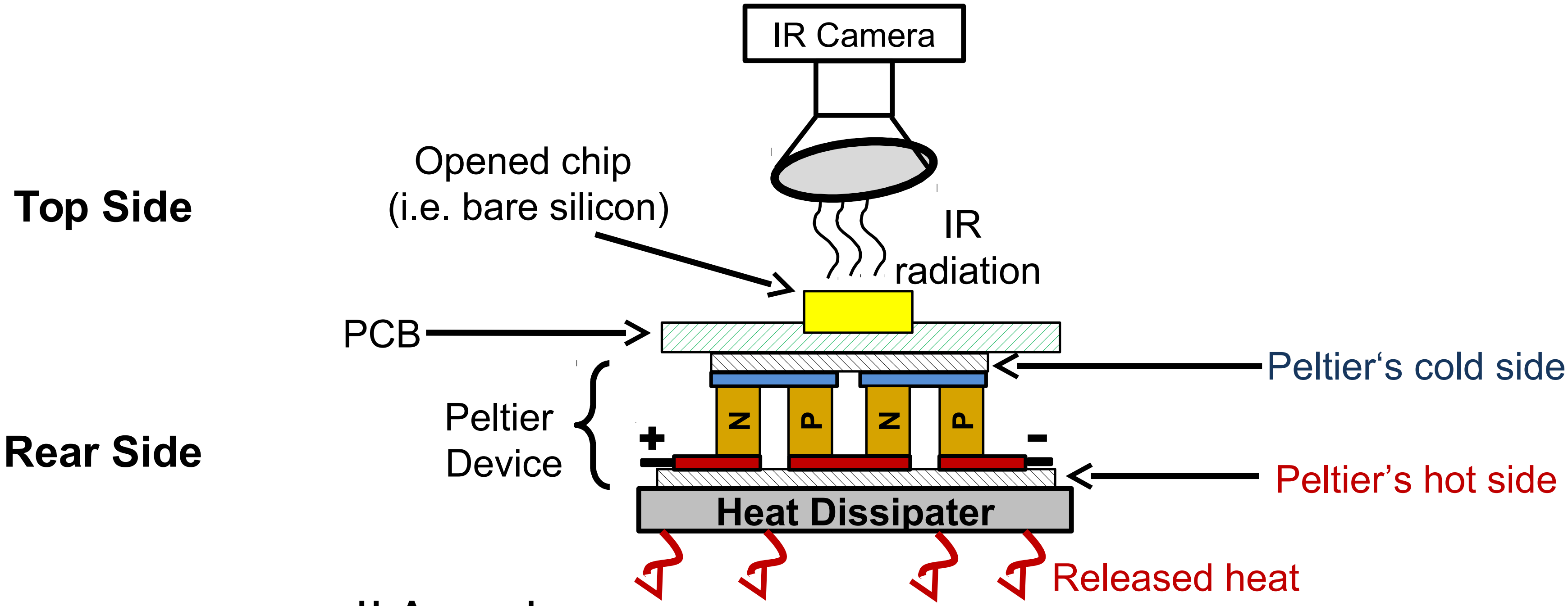




src:en.wikipedia.org

IR Thermography: Built Thermal Setup

- It continuously cools the measured chip from its rear side.
- Thermoelectric technology has been employed
  - It provides a stable/controlled source of cooling (Peltier).



src: H. Amrouch

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